

What is claimed is:

1 1. A circuit arrangement for use in communicating multiple signals over a
2 common signal path between first and second clock domains during hardware-based
3 logic emulation, wherein the first clock domain is emulated via a first multi-step
4 evaluation cycle and the second domain is emulated via a second multi-step
5 evaluation cycle, the circuit arrangement comprising:

6 (a) a buffer interposed in a common signal path between first and
7 second clock domains, the buffer including first and second locations, the first
8 location associated with a first evaluation step in the first multi-step evaluation
9 cycle and a first evaluation step in the second multi-step evaluation cycle, and
10 the second location associated with a second evaluation step in the first multi-
11 step evaluation cycle and a second evaluation step in the second multi-step
12 evaluation cycle; and

13 (b) logic circuitry coupled to the buffer, the logic circuitry configured
14 to store in the first location of the buffer a first time-multiplexed signal output
15 over the common signal path by the first clock domain during the first
16 evaluation step in the first multi-step evaluation cycle, and to store in the
17 second location of the buffer a second time-multiplexed signal output over the
18 common signal path by the first clock domain during the second evaluation
19 step in the first multi-step evaluation cycle, the logic circuit further configured
20 to output the first time-multiplexed signal stored in the first location over the
21 common signal path to the second clock domain during the first evaluation
22 step in the second multi-step evaluation cycle, and to output the second time-
23 multiplexed signal stored in the second location over the common signal path
24 to the second clock domain during the second evaluation step in the second
25 multi-step evaluation cycle.

1 2. The circuit arrangement of claim 1, wherein the buffer comprises a multi-
2 port array including a write port and a read port, and wherein the logic circuitry
3 comprises a write control circuit and a read control circuit respectively coupled to the
4 write port and read port of the multi-port array, the write control circuit configured to

5 control storage of signals from the first clock domain in the multi-port array, and the
6 read control circuit configured to control output of signals from the multi-port array to
7 the second clock domain.

1 3. The circuit arrangement of claim 2, wherein each of the write and read
2 control circuits includes a counter.

1 4. The circuit arrangement of claim 3, wherein the counter in the write control
2 circuit is configured to be incremented during each evaluation step in the first multi-
3 step evaluation cycle, and wherein the counter in the read control circuit is configured
4 to be incremented during each evaluation step in the second multi-step evaluation
5 cycle.

1 5. The circuit arrangement of claim 4, wherein the counter in the write control
2 circuit is configured to be reset for each first multi-step evaluation cycle, and wherein
3 the counter in the read control circuit is configured to be reset for each second multi-
4 step evaluation cycle.

1 6. The circuit arrangement of claim 4, wherein the counter in the first multi-
2 step evaluation cycle maintains a current evaluation step number for the first clock
3 domain, wherein the counter in the second multi-step evaluation cycle maintains a
4 current evaluation step number for the second clock domain, wherein the read and
5 write control circuits are each configured to use the respective current evaluation step
6 numbers stored in the respective counters to address the multi-port array.

1 7. The circuit arrangement of claim 1, wherein the first and second multi-step
2 evaluation cycles have different numbers of evaluation steps from one another.

1 8. The circuit arrangement of claim 1, wherein the buffer is further interposed
2 within a second common signal path between the first and second clock domains, and
3 wherein the logic circuitry is further configured to store in the buffer time-multiplexed

4 signals output over the second common signal path by the first clock domain
5 concurrently with storing time-multiplexed signals output over the first common
6 signal path, and to output over the second common signal path from the buffer to the
7 second clock domain, the time-multiplexed signals stored in the buffer.

1 9. The circuit arrangement of claim 1, wherein the first and second locations
2 are each a plurality of bits wide, wherein the buffer is interposed within a multi-bit
3 common signal path between the first and second clock domains, and wherein the
4 logic circuitry is further configured to stored in the buffer multi-bit time-multiplexed
5 signals output over the multi-bit common signal path by the first clock domain, and to
6 output over the multi-bit common signal path from the buffer to the second clock
7 domain, the multi-bit time-multiplexed signals stored in the buffer.

1 10. A logic board comprising the circuit arrangement of claim 9.

1 11. A logic emulator comprising the circuit arrangement of claim 9.

1 12. The logic emulator of claim 11, further comprising a plurality of
2 emulation processor integrated circuit devices, at least one of the emulation processor
3 integrated circuit devices configured to emulate the first clock domain, and at least
4 one other of the emulation processor integrated circuit devices configured to emulate
5 the second clock domain.

1 13. The logic emulator of claim 12, further comprising a plurality of logic
2 boards, each including a subset of the plurality of emulation processors, and wherein
3 the common signal path extends between emulation processors disposed on different
4 logic boards.

1 14. A circuit arrangement for use in communicating multiple signals over a
2 common signal path between first and second clock domains during hardware-based
3 logic emulation, wherein the first clock domain is emulated using a first multi-step
4 evaluation cycle and the second domain is emulated using a second multi-step
5 evaluation cycle, the circuit arrangement comprising:

6 (a) a buffer interposed between the first and second clock domains
7 within the common signal path, the buffer including a plurality of locations,
8 each of which associated with an evaluation step from each of the first and
9 second multi-step evaluation cycles;

10 (b) a write control circuit responsive to a first step signal associated
11 with a current evaluation step in the first multi-step evaluation cycle, the write
12 control circuit configured to store a signal output over the common signal path
13 by the first clock domain in a location in the buffer that is associated with the
14 current evaluation step in the first multi-step evaluation cycle; and

15 (c) a read control circuit responsive to a second step signal associated
16 with a current evaluation step in the second multi-step evaluation cycle, the
17 read control circuit configured to output a signal stored in a location in the
18 buffer that is associated with the current evaluation step in the second multi-
19 step evaluation cycle.

1 15. The circuit arrangement of claim 14, wherein the buffer comprises a
2 multi-port array including a write port coupled to the write control circuit and a read
3 port coupled to the read control circuit, wherein the write control circuit includes a
4 counter configured to be incremented in response to the first step signal, and wherein
5 the read control circuit includes a counter configured to be incremented in response to
6 the second step signal.

1 16. The circuit arrangement of claim 15, wherein the counter in the write
2 control circuit is configured to be reset for each first multi-step evaluation cycle, and
3 wherein the counter in the read control circuit is configured to be reset for each second
4 multi-step evaluation cycle.

1 17. The circuit arrangement of claim 15, wherein the counter in the first multi-
2 step evaluation cycle maintains a current evaluation step number for the first clock
3 domain, wherein the counter in the second multi-step evaluation cycle maintains a
4 current evaluation step number for the second clock domain, wherein the read and
5 write control circuits are each configured to use the respective current evaluation step
6 numbers stored in the respective counters to address the multi-port array.

1 18. The circuit arrangement of claim 14, wherein the first and second multi-
2 step evaluation cycles have different numbers of evaluation steps from one another.

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1 19. A method of communicating multiple signals over a common signal path
2 between first and second clock domains during hardware-based logic emulation, the
3 method comprising:

4 (a) during each of a first plurality of evaluation steps in an evaluation
5 cycle for the first clock domain, communicating a signal associated with such
6 evaluation step across the common signal path from the first clock domain to a
7 buffer that has a plurality of locations, and storing the communicated signal in
8 a location among the plurality of locations in the buffer that is associated with
9 such evaluation step; and

10 (b) during each of a second plurality of evaluation steps in an
11 evaluation cycle for the second clock domain, wherein each of the second
12 plurality of evaluation steps is associated with a location among the plurality
13 of locations, communicating a signal from the location in the buffer that is
14 associated with such evaluation step from the second plurality of evaluation
15 steps to the second clock domain.

1 20. The method of claim 19, wherein communicating the signal associated
2 with each evaluation step in the evaluation cycle for the first clock domain includes
3 incrementing a first counter for each such evaluation step, and wherein
4 communicating the signal from the location associated with each evaluation step in
5 the evaluation cycle for the second clock domain includes incrementing a second
6 counter for each such evaluation step.

1 21. The method of claim 20, further comprising resetting the first counter for
2 each evaluation cycle for the first clock domain, and resetting the second counter for
3 each evaluation cycle for the second clock domain.

1 22. A method of communicating multiple signals over a common signal path
2 between first and second clock domains during hardware-based logic emulation,
3 wherein the first clock domain is emulated via a first multi-step evaluation cycle that
4 includes first and second evaluation steps and the second domain is emulated via a
5 second multi-step evaluation cycle that includes first and second evaluation steps, the
6 method comprising:

7 (a) during the first evaluation step in the first multi-step evaluation
8 cycle, receiving a first time-multiplexed signal output over the common signal
9 path by the first clock domain and storing the first time-multiplexed signal in a
10 first location in a buffer interposed in the common signal path, wherein the
11 first location is associated with the first evaluation step in the first multi-step
12 evaluation cycle and the first evaluation step in the second multi-step
13 evaluation cycle;

14 (b) during the second evaluation step in the first multi-step evaluation
15 cycle, receiving a second time-multiplexed signal output over the common
16 signal path by the first clock domain and storing the second time-multiplexed
17 signal in a second location in the buffer, wherein the second location is
18 associated with the second evaluation step in the first multi-step evaluation
19 cycle and the second evaluation step in the second multi-step evaluation cycle;

20 (c) during the first evaluation step in the second multi-step evaluation
21 cycle, communicating the first time-multiplexed signal stored in the first
22 location over the common signal path to the second clock domain; and

23 (d) during the second evaluation step in the second multi-step
24 evaluation cycle, communicating the second time-multiplexed signal stored in
25 the second location over the common signal path to the second clock domain.
26

1 23. The method of claim 22, wherein the buffer comprises a multi-port array
2 including a write port and a read port, the method further comprising incrementing a
3 first counter for each evaluation step in the first multi-step evaluation cycle,
4 incrementing a second counter for each evaluation step in the second multi-step

5 evaluation cycle, and utilizing the first and second counters to respectively address the
6 write and read ports of the multi-port array.

1 24. The method of claim 20, further comprising resetting the first counter for
2 each first multi-step evaluation cycle, and resetting the second counter for each second
3 multi-step evaluation cycle.

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